NBR-003-027804 Seat No. _____

M. Sc. (ECI) (Sem. VIII) (CBCS) Examination

April / May – 2017

Paper - 32 : VHDL : Fundamentals & Practice (New Course)

Faculty Code : 003
Subject Code : 027804

Time : $2\frac{1}{2}$ Hours] [Total Marks : **70**

Instructions :

(1) All questions carry equal compulsory.
(2) Figures on right hand side indicate marks.

1 Answer the following : (any **seven**) **14**

(1) What is VHDL ?
(2) Write about Library declaration in VHDL.
(3) Write the syntax of "ARCHITECTURE" of VHDL code.
(4) Make a list of Pre-defined data types of VHDL.
(5) Define. Array in VHDL.
(6) Define d'RIGHT and d'LENGTH data attributes of VHDL.
(7) What is sequential logic in'VHDL ?
(8) Define PROCESS section of VHDL code.
(9) Write difference between Signal and Variable of VHDL.
(10) What is state machine ?

2 Answer the following : (any **two**) **14**

(1) Explain fundamental VHDL units and design flow of VHDL. **7**
(2) Write a VHDL code for' Multiplexer. **7**
(3) Write a VHDL code of 4-bit Adder with one output (sum) for both SIGNED and INTEGER datatypes. **7**

3 Answer the following : 14

(1) Explain STD_LOGIC, STD_ULOGIC, BOOLEAN, INTEGER, SIGNED, UNSIGNED data types of VHDL. 7

(2) Explain Assignment, Logical and Shift operators of VHDL. 7

OR

3 Answer the following : 14

(1) Write a note on combinational versus sequential logic. 7

(2) Explain GENERATE statement with example. 7

4 Answer the following : 14

(1) Write a VHDL program for 1-digit decimal counter ($0 \rightarrow 9 \rightarrow 0$), according to top-level diagram shown in **fig. (a)**. 7

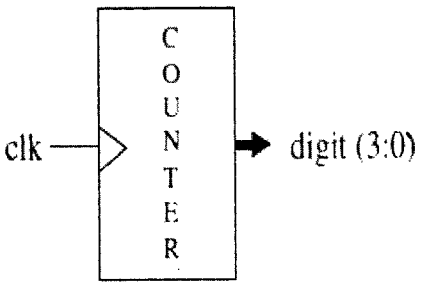

Fig. (a)

(2) Explain FOR/LOOP, WHILE/LOOP, NEXT, EXIT with examples. 7

5 Answer the following : (any **two**) 14

(1) Write a VHDL code for D-Flip-flop with output Q and Qbar. 7

(2) Explain Mealy State Machine with diagram. 7

(3) Write a VHDL program for GENERIC 3:8 Decoder. 7

(4) Write a VHDL program for Encoder. 7